the patent warranted hereon all changes and modifications as reasonably and properly come within the scope of their contribution to the art.–.

IN THE CLAIMS:

Please cancel claims 1-5 and substitute the following claims 6-10 therefor:

6. A method for the production of a vertical MOS transistor, said method comprising the steps of:

forming a mask of an insulating material on a main surface of a semiconductor substrate, said mask having a first opening therethrough exposing said main surface of said semiconductor substrate;

forming a layer sequence of sequentially a lower source/drain region, a channel region, and an upper source/drain region in said first opening by selective epitaxy with facets being formed on an edge of said layer sequence for said layers to have a lesser thickness at an edge of said first opening than at a middle of said opening;

after forming said layer sequence, exposing a side wall of said channel region with a side wall of said lower source/drain region remaining essentially covered by said insulating material of said mask;

forming a gate dielectric at said exposed side wall of said channel region and adjoining a surface of said channel region; and

forming a gate electrode adjoining said gate dielectric.

7. The method according to claim 6, wherein said mask comprises at least one material selected from the group consisting of silicon oxide and silicon nitride, said mask comprising said at least one material at least at a surface of said mask.

8. The method according to claim 6,

wherein the step of forming a mask comprises the steps of:

forming a first insulating layer on said main surface; and

forming a second insulating layer on said first insulating layer, said second insulating layer being etched selectively with respect to said first insulating layer and to said layer sequence;

wherein the step of forming a layer sequence comprises forming said lower source/drain region essentially level with said first insulating layer; and

said method further comprising the steps of:

forming a second opening annularly surrounding said channel region in said second insulating layer;

after forming said gate dielectric, filling said second opening with a conductive layer; and

wherein the step of forming said gate electrode comprises structuring said conductive layer.

9. The method according to claim 8,

wherein said second opening comprises an extension at at least one side of said layer sequence, said extension of said second opening having a grid-like cross-section from island like structures arranged therethrough; and

wherein said conductive layer filling said second opening further fills said extension of said second opening.

10. The method according to claim 6, further comprising the steps of:

structuring said layer sequence in an annular shape; and

providing said annularly structured layer sequence with an insulating filling.